REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 31-52 are in this application. Claims 1-30 have been cancelled. Claims 31-32, 37-38, 40, 42-43, 48-49, and 51 have been amended. In addition to the amendments discussed below, the claims have been amended to alternately claim the invention.

The Examiner rejected claims 31-36, 38-39, 42-47, and 49-50 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Patent No. 6,162,368). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 31 recites, in part,

> "forming a layer of first material to contact the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first region and a second region that lies above the first region of the layer of first material, the first region of the layer of first material being equal to a lowest part of the top surface of the layer of first material, the second region of the layer of first material being equal to a highest part of the top surface of the layer of first material;
>
> "forming a layer of second material to contact the top surface of the layer of first material, the layer of second material having a top surface, the top surface of the layer of second material having a first region and a second region that lies above the first region of the layer of second material, the first region of the layer of second material being equal to a lowest part of the top surface of the layer of second material, the second region of the layer of second material being equal to a highest part of the top surface of the layer of second material, the first region of the top surface of the layer of second material lying above the second region of the top surface of the layer of first material."

In rejecting the claims, the Examiner pointed to polysilicon layer 16 shown in FIG. 2A of the Li reference as constituting the layer of first material required by the claims, and native oxide layer 18 shown in FIG. 2A of the Li reference as

constituting the layer of second material. The Li reference, however, totally fails to teach or suggest that the first region of the top surface of the layer of second material lies above the second region of the top surface of the layer of first material.

As shown in FIG. 2A of the Li reference, the lowest portion of the top surface of native oxide layer 18 does not lie above the highest portion of the top surface of polysilicon layer 16 as required by claim 31, but instead lies below the highest portion of the top surface of polysilicon layer 16. As a result, native oxide layer 18 can not be read to be the layer of second material required by claim 31.

Thus, since the Li reference fails to teach or suggest a layer of second material that has a first region of the top surface that lies above a second region of the top surface of the layer of first material, claim 31 is not anticipated by the Li reference. In addition, since claims 32-36 and 38-39 depend either directly or indirectly from claim 31, these claims are not anticipated by Li for the same reasons as claim 31.

Claim 31 also recites:

> "performing a chemical-mechanical polish of the layer of second material and the layer of first material, the chemical-mechanical polish continuing until the layer of second material has been substantially all removed from the layer of first material, thereby forming the layer of first material to have a substantially planar top surface, the substantially planar top surface of the layer of first material lying over the first region and the second region of the top surface of the wafer."

As noted above, the Examiner pointed to polysilicon layer 16 shown in FIG. 2A of Li as constituting the layer of first material required by the claims, and native oxide layer 18 shown in FIG. 2A of Li as constituting the layer of second material. The Examiner also pointed to the chemical-mechanical polishing steps shown in

FIGS. 2D-2F of Li as constituting the chemical-mechanical polishing element required by the claims.

As shown in FIGS. 2B-2C, Li teaches that native oxide layer 18 (read to be the layer of second material) is chemically-mechanically polished to remove native oxide layer 18 from polysilicon layer 16 (read to be the layer of first material). However, FIGS. 2B-2C of Li totally fail to teach or suggest that the polishing continues until substantially all of native oxide layer 18 has been removed, thereby forming polysilicon layer 16 to have a substantially planar top surface as required by claim 31.

The term "until" is a function word that indicates continuance of an action to a specified time. (See http://www.m-w.com/dictionary/until - copy attached in Appendix A.) Thus, claim 31 requires that the chemical-mechanical polish continue to a specified time, which is the removal of substantially all of the layer of second material. At this point, the action (the chemical-mechanical polish) stops.

In addition, the term "thereby" means "by that". (See http://www.m-w.com/dictionary/thereby - copy attached in Appendix B.) Thus, claim 31 requires that, by the chemical-mechanical polish which stops when substantially all of the layer of second material has been removed, the layer of first material is formed to have a substantially planar top surface.

Li teaches:

> "[a]s shown by FIGS. 2B and 2C, the brief polishing at polishing station 25a with oxide-polishing slurry 50a is sufficient to remove native oxide layer 18 from the substrate surface. Referring to FIGS. 2C and 2D, once the native oxide layer has been removed, the substrate is polished with polysilicon-polishing slurry 50b. This polishing continues until polysilicon layer 16 is partially or substantially planarized, i.e., the large scale topography such as the peaks and valleys have been substantially removed." [Underlining added.] (See from column 5, line 64 to column 6, line 6 of Li.)

Thus, if the Li reference is read as teaching that native oxide layer 18 (read to be the layer of second material) is polished with slurry 50a until substantially all of native oxide layer 18 has been removed (at which time slurry 50b is used), then Li fails to teach or suggest that polishing with slurry 50a thereby forms polysilicon layer 16 (read to be the layer of first material) to have a substantially planar top surface.

As shown in FIG. 2C of Li, once native oxide layer 18 has been removed, polysilicon layer 16 has a severely non-planar top surface. As a result, it is not possible for native oxide layer 18 to be polished until native oxide layer 18 has been substantially all removed, thereby forming polysilicon layer 16 to have a substantially planar top surface.

Claim 42 recites, in part,

> "performing a chemical-mechanical polish of the layer of second material and the layer of first material, the chemical-mechanical polish continuing until the layer of second material has been substantially all removed from the layer of first material at which time the layer of first material has a substantially planar top surface, the substantially planar top surface of the layer of the layer of first material lying over the second region of the top surface of the wafer."

As noted above, as shown in FIGS. 2B-2C, Li teaches that native oxide layer 18 (read to be the layer of second material) is chemically-mechanically polished to remove native oxide layer 18 from polysilicon layer 16 (read the layer of first material). However, FIGS. 2B-2C, Li totally fail to teach or suggest that the polishing continues until substantially all of native oxide layer 18 has been removed at which time polysilicon layer 16 has a substantially planar top surface as required by claim 42.

Thus, if the Li reference is read as teaching that native oxide layer 18 (read to be the layer of second material) is polished with slurry 50a until substantially all of native oxide layer 18 has been removed (at which time slurry 50b is used), then Li fails to teach or suggest that, "at which time" substantially all of native oxide layer 18 has been removed, polysilicon layer 16 has a substantially planar top surface.

As noted above, once native oxide layer 18 has been removed as shown in FIG. 2C of Li, polysilicon layer 16 has a severely non-planar top surface. As a result, it is not possible for native oxide layer 18 to be polished until native oxide layer 18 has been substantially all removed at which time polysilicon layer 16 has a substantially planar top surface.

In the present Response to Arguments section, the Examiner pointed to FIG. 2D of Li and appears to argue that polysilicon layer 16 (read to be the layer of first material) is polished to have a planar surface prior to the use of slurry 50b and polishing pads 104 and 106. Applicant respectfully does not understand the Examiner's argument as FIG. 2C of Li shows the use of slurry 50b and polishing pads 104 and 106 before polysilicon layer 16 has been polished to have a planar surface, and while polysilicon layer 16 still has a severely non-planar top surface.

The Examiner also argued that the removal of native oxide layer 18 (read to be the layer of second material) and the planarizing of polysilicon layer 16 (read to be the layer of first material) occur concurrently within a short period of time. Applicant respectfully notes that it is irrelevant whether native oxide layer 18 and any portion of polysilicon layer 16 are removed at the same time.

Even if is assumed that native oxide layer 18 (read to be the second material layer) and a portion of polysilicon layer 16 (read to be the layer of first material) are removed at the same time, FIG. 2C of Li shows that when substantially all of

native oxide layer 18 has been removed, polysilicon layer 16 does not have a substantially planar top surface.

In addition, the Examiner argued that the present application does not disclose that the chemical-mechanical planarizing (CMP) process of the present invention produces a planar surface that can not be achieved by the CMP process of Li. However, applicant's specification does disclose that the CMP process of the present invention produces a planar surface that can not be achieved by the CMP process of Li.

Applicant notes that the Li reference teaches that under polishing results in a "center slow effect", which is the tendency of the substrate center to be polished more slowly that the substrate edge. If the polishing parameters are changed to increase the amount of material removed from the substrate center, then the outer portion will be over polished. (See column 1, lines 44-58 of Li.)

As stated in Li, it is believed that the "center slow effect" is caused by the presence of native oxide layer 18, which is extremely thin and on the order of a few atomic layers. (See column 4, lines 58-63 of Li.) The approach in Li is to first remove the very thin native oxide layer 18, and then begin planarizing the severely non-planar top surface of polysilicon layer 16.

However, once Li begins to planarize the severely non-planar top surface of polysilicon layer 16, Li is subject to the same thinning problems as discussed in applicant's specification from page 2, line 6 to page 3, line 9, and illustrated in applicant's prior-art FIG. 2B with arrows A and B. As disclosed in applicant's specification, the present invention reduces the problems of thinning by utilizing a substantially thicker layer of oxide. (See page 2, lines 18-28 and page 6, lines 20-24 of applicant's specification.) Thus, applicant's specification does disclose that the CMP process of the present invention produces a planar surface that can not be achieved by Li.

As a result, the chemical-mechanical polishing taught by Li can not be read to be the chemical-mechanical polish required by the claims. Therefore, since the Li reference does not teach or suggest the chemical-mechanical polish element required by claims 31 and 42, claims 31 and 42 are not anticipated by Li. In addition, since claims 32-36 and 38-39 depend either directly or indirectly from claim 31, these claims are not anticipated by Li for the same reasons as claim 31. Further, since claims 43-47 and 49-50 depend either directly or indirectly from claim 42, claims 43-47 and 49-50 are not anticipated by Li for the same reasons as claim 42.

With further respect to claims 38 and 49, these claims have been amended to further prosecution, and recite:

> "forming a layer of third material over the substantially planar top surface of the layer of first material, the third layer of material lying above and being vertically spaced apart from the second region of the top surface of the wafer."

Claim 49 recites the same limitations.

In rejecting the claims, the Examiner pointed to FIGS. 2A-2I, and the text from column 4, line 37 to column 6, line 54 of Li as teaching the formation of a third layer of material. In the Response to Arguments section, the Examiner pointed to FIG. 2I of Li and argued that polishing pad 110 (114) can be read to be the third layer of material.

Applicant notes, however, that polishing pad 110 (114) is not formed over the polished layer of material, but instead is placed over the polished combination of insulative layer 14 and polysilicon layer 16 shown in FIG. 2I of Li. One skilled in the art would not understand the placement of a polishing pad to be the formation of a layer of material. Thus, since one skilled in the art would not understand the

placement of a polishing pad to be the formation of a layer of material, claims 38 and 49 are not anticipated by Li for this additional reason.

With further respect to claims 39 and 50, these claims recite "wherein the layer of third material is a mask." In the Response to Arguments Section, the Examiner argued that the term "mask" does not have any special meaning because applicant does not define what the mask layer entails or represents in terms of its function and usage. Applicant, however, is not arguing that the term "mask" be given any special meaning, but that the term "mask" be given its usual and customary meaning in the semiconductor art.

The Examiner further argued that the term "mask" has a very broad interpretation and function in the semiconductor industry, and that a polishing pad is analogous to a mask for a CMP process. The Examiner then requested that applicant supply evidence that the function of a mask is different from the function of a polishing pad.

The definition of a mask in the semiconductor art is "[a] protective mask that is a thin template of metal or another material used to shield parts of a semiconductor during an etching or deposition process." (See http://www.intota.com/multisearch.asp?strSearchType=all&strQuery=semiconductor+mask - copy attached in Appendix C.) Thus, since a polishing pad does not shield part of a semiconductor during an etching or deposition process, a polishing pad can not be interpreted to be a mask. Therefore, since a polishing pad can not be read to be a mask, claims 39 and 50 are not anticipated by Li for this reason as well.

The Examiner also rejected claims 37 and 48 under 35 USC §103(a) as being unpatentable over Li et al. in view of Weling et al. (U.S. Patent No. 5,378,318). In rejecting the claims, the Examiner argued that Li teaches all of the claimed limitations except for a specific etch selectivity. However, as noted above, the Li et

al. reference does not teach all of the claimed limitations. As a result, claims 37 and 48 are patentable over the Li et al. reference in view of the Weling et al. reference for the same reasons that claims 31 and 42 are not anticipated by the Li et al. reference.

The Examiner further rejected claims 40-41 and 51-52 under 35 USC §103(a) as being unpatentable over Li et al. in view of Sandhu et al. (U.S. Patent No. 5,381,302). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 40 recites:

> "the substantially planar top surface of the layer of first material includes doped polysilicon; and
> "the layer of third material lowers a resistance of doped polysilicon."

Claim 51 recites the same limitations.

In rejecting the claims, the Examiner noted that Li does not specifically disclose that the layer of third material lowers a resistance of polysilicon, but pointed to Sandhu as teaching the formation of a metallic layer 62 over a polysilicon layer 65 to lower the sheet resistance of the polysilicon layer. The Examiner then argued that one skilled in the art would have been motivated to form a metal layer over the polysilicon layer to reduce the sheet resistance of the polysilicon layer.

Applicant respectfully notes, however, that the Examiner has not read a polysilicon layer to be the third layer of material, but instead has read polishing pad 110 (114) to be the third layer of material. Applicant has been unable to find anything in Sandhu that teaches or suggests that polishing pad 110 (114) lowers a resistance of doped polysilicon. Thus, since Sandhu does not teach or suggest that a polishing pad lowers the resistance of polysilicon, claims 40 and 51 are

patentable over Li in view of Sandhu. In addition, since claims 41 and 52 depend directly from claims 40 and 51, respectively, claims 41 and 52 are patentable over Li in view of Sandhu for the same reasons that claims 40 and 51 are patentable over Li in view of Sandhu.

With further respect to claims 41 and 52, these claims recite "forming a mask on the layer of third material." In rejecting the claims, the Examiner pointed to Sandhu as teaching the formation of a mask over the metal layer (titanium) to keep the titanium over the polysilicon plug, while removing the titanium from the portion of the ILD layer.

Applicant respectfully notes, however, that the Examiner has read polishing pad 110 (114) to be the third layer of material. Applicant has been unable to find anything in Sandhu that teaches or suggests forming a mask on polishing pad 110 (114). Thus, claims 41 and 52 are patentable over Li in view of Sandhu for this additional reason.

Thus, for the foregoing reasons, it is submitted that the application is in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

Dated: 8-21-06 By: Mark C. Pickering

Mark C. Pickering
Registration No. 36,239
Attorney for Assignee

P.O. Box 300
Petaluma, CA 94953-0300
Telephone: (707) 762-5500
Facsimile: (707) 762-5504
Customer No. 33402

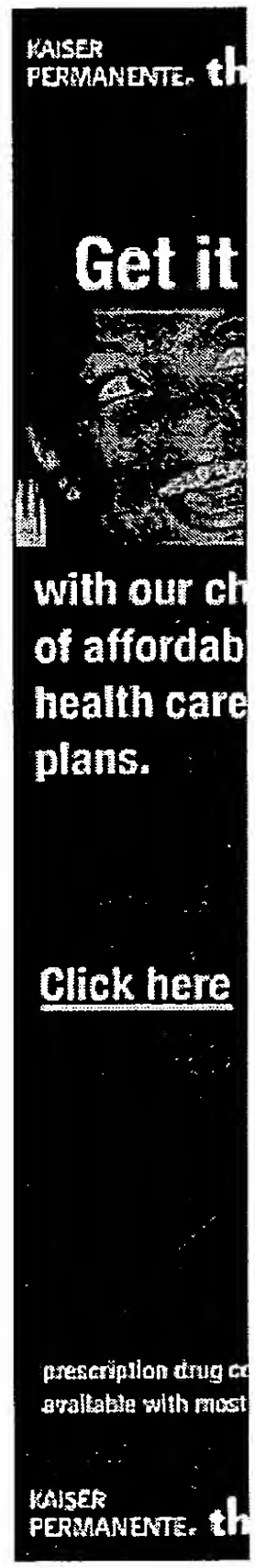
APPENDIX A

until

2 entries found for **until**.
To select an entry, click on it.

until[1,preposition]
until[2,conjunction]
Go

Main Entry: [1]**un·til**
Pronunciation: `&n-'til, -'tel; '&n-", -t&l`
Function: *preposition*
Etymology: Middle English, from *un-* (probably from Old Norse **und* up to; akin to Old Norse *unz* up to, until, Old High German *unt,* Old English *ende* end) + *til, till* till
1 *chiefly Scottish* **:** **TO**
2 -- used as a function word to indicate continuance (as of an action or condition) to a specified time <stayed *until* morning>
3 : **BEFORE** 2 <not available *until* tomorrow> <we don't open *until* ten>



APPENDIX B

Merriam-Webster Online Dictionary

thereby

One entry found for **thereby**.

Main Entry: **there·by**
Pronunciation: [th]er-'bI, '[th]er-"
Function: *adverb*
1 : by that **:** by that means <*thereby* lost her chance to win>
2 : connected with or with reference to that <*thereby* hangs a tale -- Shakespeare>

For **More Information on "thereby" go to Britannica.com**
Get the **Top 10 Search Results for "thereby"**

APPENDIX C

intota™

Expert Consulting and Expert Witness Services

Experts in 'semiconductor mask'

Definition: A protective mask that is a thin template of metal or another material used to shield parts of a semiconductor during an etching or deposition process.

Related Search Terms
- hard semiconductor mask
- soft semiconductor mask
- semiconductor mask
- contact aligner
- photoresist
- semiconductor lithography
- microlithography
- semiconductor device
- etching
- semiconductor material processing
- semiconductor sililation
- photoresist stripping
- semiconductor wafer mask aligner
- semiconductor dopant lateral diffusion
- ion-beam etching
- etch pit density
- etching material
- etch rate
- photochemical etching
- lift-off (semiconductor fabrication)

Experts - 1 to 6 of 6	Expertise	View Bio	Request a Project
Expert 107629	Scanning Electron and Light Microscopy, EBEAM Lithography and Nanofabrication	View Bio	Request a Project
Expert 720603	Semiconductor Processing and Equipment	View Bio	Request a Project
Expert 722748	Advanced Semiconductor Technology Intellectual Property and Licensing	View Bio	Request a Project
Expert 108092	Semiconductor Manufacturing	View Bio	Request a Project
Expert 107923	Semiconductor Processing Technology	View Bio	Request a Project
Expert 713180	Lithographic Printing Plates, Ink Jet Imaging and CTP Technology	View Bio	Request a Project

Can't find the right expert in 'semiconductor mask'? We can help!